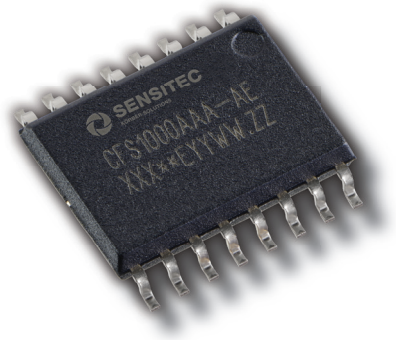
SENSITEC
KÖRBER SOLUTIONS

DATA SHEET

CFS1000

Integrated MagnetoResistive Current Sensor



The CFS1000 current sensor is designed for highly dynamic electronic measurements of DC, AC, or pulsed currents with integrated galvanic isolation. This current sensor based on the Anisotropic MagnetoResistive (AMR) effect enables excellent dynamic response without the hysteresis present in designs using ironcores. The primary current measured needs to be fed below the sensor on PCB or current rail. Usually a U-shaped conductor is applied to define the magnetic field gradient needed to excite the sensor.

The sensor device includes a high-precision sensor signal conditioner IC providing internal feedback of a compensation current for optimum linearity. The IC output is an offset calibrated and pre-scaled current which is proportional to the primary current measured. This output is easily converted to a voltage with an external resistor at the post-processing device (usually ADC or amplifier). A precise on-chip voltage reference is generated. Alternatively, an external reference can be used. Total accuracy of a multi-sensor system is improved by sharing one voltage reference for all sensors. Additionally, a fast overcurrent alarm output allows immediate reaction to overload events independent of controller and software.

Product Overview

Article Description	Package	Delivery Type
CFS1000AAA-AE	SOIC16w (300 mil)	Tape on reel

Quick Reference Guide

Parameter	Description	Min.	Typ.	Max.	Unit
V_{SUP}	Supply voltage	4.75	5.0	5.25	V
I_{PN}	Primary nominal current (RMS) [1]	10		1000	A
I_{out}	Output current at I_{PN}		2		mA
f_{co}	Upper cut-off frequency (-3 dB)		500		kHz
ε_{Σ}	Overall accuracy [2] (T = 25 °C; calibrated)			±1.3	%
$T_{\varepsilon\Sigma}$	Overall accuracy [2] (T = -40 °C to +125 °C; calibrated)			±2	%
T_{amb}	Ambient temperature	-40		+125	°C

1) Primary nominal current range is defined by the geometry of the external primary current bar. As measuring range threefold absolute nominal current is guaranteed, restricted to 50ms, duty cycle < 1:100.

2) Overall accuracy error includes offset, linarity and sensitivity error ($\varepsilon_{\Sigma} = \varepsilon_{G} + \varepsilon_{off} + \varepsilon_{lin}$).

Qualification Overview

Standard	Name	Status
AEC-Q100 Rev-H, Grade 1	Failure mechanism based stress test qualification for integrated circuits	Approved
2011/65/EU	RoHS-conformity	Approved

Features and Benefits

- **AEC-Q100 Rev-H, Grade 1 qualified**
- Based on Anisotropic MagnetoResistive (AMR) effect
- Galvanic isolation: Contactless current sensing
- Differential field measurement: High immunity to magnetic stray fields
- High bandwidth current measurement: DC to 500 kHz
- Very fast response time: smaller 1 µs
- Coreless measurement: Negligible output hysteresis
- Excellent accuracy
- Factory programmed zero-offset temp-coefficient
- Internal precision reference or external reference input
- Fast overcurrent detection with tunable threshold

Main Application Fields

- Electrical motor controls, AC variable speed drives
- Power inverters
- Photovoltaics (micro-inverters)
- Switch mode power supplies (SMPS)
- Current measurement for safety switch control
- Battery management

ESD

RoHS-Compliant www.sensitec.com

1 Introduction

1.1 Block Diagram and typical operating circuit

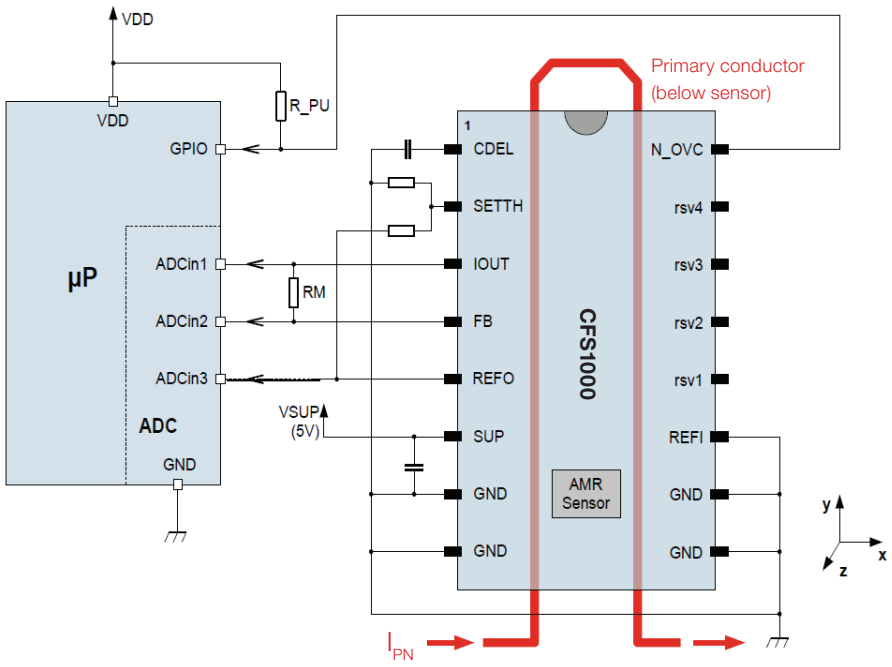


Fig. 1-1: Application example using internal reference. For the indicated primary current flow direction, V(IOUT) - V(FB) > 0.5 · V_{SUP}

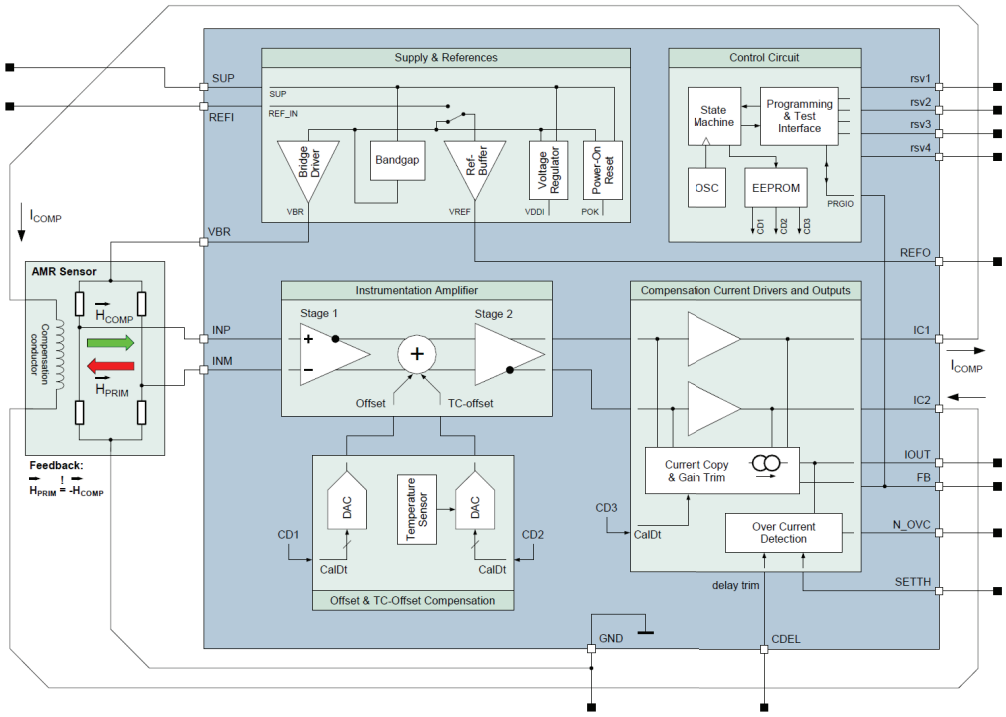


Fig. 1-2: Simplified functional block diagram: AMR-sensor + signal conditioner-IC

1.2 Brief Functional Description

The CFS1000 represents a precision current sensing device for contactless measurement using a sensor element based on the Anisotropic MagnetoResistive (AMR) effect. The device comprises the AMR-sensor, a signal-conditioning IC and supplementary components for magnetic biasing of the sensor in an SO16w package. The primary current for measurement needs to be fed below the sensing element in a well defined geometrical current path. The magnetic field gradient (component in x-direction, see Figure 1-1) is the physical quantity which directly stimulates the AMR sensor. To enable an optimum design of the primary current path a detailed documentation and a design tool is available via Sensitec's internet page (www.sensitec.com).

By integration of the sensor electronics inside a molded plastic package a high isolation voltage (>1 kV) with respect to the primary current conductor is achieved, which will be further increased by the PCB between sensor package and primary conductor.

Due to the physical characteristics and the mechanical construction of the sensor, this integrated sensor boasts with negligible hysteresis and low variance of sensitivity to mechanical displacements without the need of magnetic field concentrators. For precise sensitivity calibration the device is prepared for final end-of-line gain trimming (sensor device mounted in a fixed position with respect to the primary conductor).

The signal conditioning ASIC (Figure 1-2) comprises an input amplifier, a differential compensation current driver, a current copy circuit generating the sensor output, trimming stages for offset, offset-TC (temperature coefficient) and gain (sensitivity), calibration interface and non-volatile memory (NVM) as well as supporting circuit modules. A low noise, low offset instrumentation amplifier with high bandwidth amplifies the differential input from the AMR-bridge. Measurement of the on-chip temperature is used as an input of the compensation circuit to suppress the thermal offset drift of the AMR-bridge. This offset drift is already calibrated during factory programming of each device in multiple temperature test steps. Additionally, absolute offset errors (from sensor and amplifier) are compensated by appropriate trimming structures in this amplifier stage. Trimming can be performed either during IC factory test or in the final application. The instrumentation amplifier output is passed to a differential current output driver generating the compensation current to the sensor. This compensation current (at pins IC1, IC2) is fed back to the secondary current input of the AMR-sensor bridge. As a consequence of the feedback principle with high loop-gain an excellent linearity of the sensor is achieved because the resistive bridge always operates close to 0 mV.

The sensor output is a precise copy of the compensation current. Proper trimming of the measurement sensitivity is achieved by calibration of the current gain of this current-copy output stage. Usually, this final calibration step is performed in the application after assembling the sensor device CFS1000 with the primary current conductor. For permanent storage of the digital calibration data an E^2PROM as a non-volatile memory is included in the sensor IC. For transfer of calibration data between IC and the external calibration hardware an asynchronous programming interface via pin FB is integrated, which can be accessed in a defined time window after power-on of the device.

As a fast overcurrent monitor a comparator supervises the sensor output and signals the status at pin N_OVC. This output is pulled to digital low level whenever the measured current (corresponding to the absolute value at IOUT) exceeds a fraction of the full-scale range defined by the voltage level at SETTH.

Further blocks of the ASIC are reference voltage and reference current generators, the stabilized supply to the sensor bridge and a stabilized supply voltage to the internal blocks. A buffered voltage reference output is provided at pin REFO which is connected either to the precise internal voltage reference (2.5 V) or an external reference input REFI. With pin REFI at low level (connected to ground) the internal reference is available at pin REFO and with REFI above a decision threshold, this input voltage is copied to output pin REFO. Also a power-on reset circuit is integrated to suppress any invalid or disturbed sensor output in case of supply voltage V_{SUP} out of its specified range.

2 Package Information

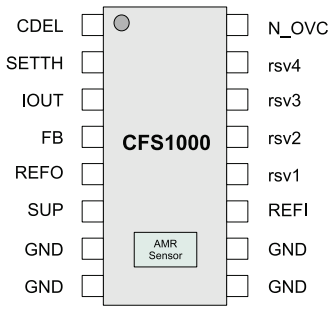
2.1 Plastic Package

The product is available in a Pb free, RoHS compliant, 16 lead Small Outline Wide plastic package (SO16w, 300 mil) with about 106 mm² (0.165 square inch) footprint area. For dimension details refer to JEDEC standard MS-013-F, version AA.

The device has been classified for MSL 3 according to JEDEC J-STD-020 for the following soldering profile:

– (260±5) °C, dwell time <10 s

2.2 Pin Configuration



Note:
The magnetically sensitive area of the device is centered on the virtual connecting line between pins 7 and 10 of the package (see also figure 7-1).

Fig. 2-1: Pinout (not to scale).

2.3 Pin Description

Pin No.	Pin Name	Type [1]	Description	Remark
1	CDEL	A I O	Delay setting capacitor for overcurrent detection	
2	SETTH	A I	Threshold setting input for overcurrent detection	
3	IOUT	A O	Current output signal	
4	FB	A I	Feedback pin for current output IOUT; in programming mode IC digital IO of ASIF	Connect shunt resistor to IOUT
5	REFO	A O	Reference voltage output	
6	SUP	S	Supply (5 V)	
7	GND	S	Ground connection	Multiple ground pins (7 - 10)
8	GND	S	Ground connection	
9	GND	S	Ground connection	
10	GND	S	Ground connection	
11	REFI	A I	Reference select / reference voltage input	Connect to GND for internal reference
12	rsv1	D I	Internally connected. Reserved for factory use	[2) 3)]
13	rsv2	-	Internally connected. Reserved for factory use	Leave open!
14	rsv3	D I	Internally connected. Reserved for factory use	[2) 3)]
15	rsv4	-	Internally connected. Reserved for factory use	[2)]
16	N_OVC	D O	Overcurrent alarm output; open drain driver	Low active (high-resistive pull-up integrated)

[1] D = digital, A = analog, S = Supply, I = Input, O = Output.

[2] Recommend to be connected to GND in the application, may be left open.

[3] Optionally used in application programming, see section 6.6.2.

3 Absolute Minimum/Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

All voltages referred to V(GND). Currents flowing into terminals are positive, those drawn out of a terminal are negative.

No.	Parameter	Description	Min.	Max.	Unit	Condition
1	V_{SUP}	Supply voltage	-0.3	+6.5	V	
2	V_{DPIN}	Voltage at digital I/O pins rsv1, rsv3	-0.3	V_{SUP} + 0.3	V	
3	I_{DPIN}	Input current at digital pins rsv1, rsv3	-20	+20	mA	
4	V_{N_OVC}	Voltage at digital open drain output N_OVC	-0.3	V_{SUP} + 0.3	V	
5	I_{N_OVC}	Current at open drain output OVC	-20	+20	mA	Output driver off
6	V_{APIN}	Voltage at analog pins IOUT, FB, REFO, SETTH, CDEL	-0.3	V_{SUP} + 0.3	V	
7	I_{APIN}	Input current at analog pins IOUT, FB, REFO, SETTH, CDEL	-20	+20	mA	
8	V_{REFI}	Voltage at pin REFI	-0.3	8.0	V	
9	I_{REFI}	Input current at pin REFI	-20	+2	mA	
10	T_J	Junction temperature	-40	+150	°C	
11	T_{AMB}	Ambient temperature	-40	+125	°C	Packaged in SO16w
12	T_{STG}	Storage temperature [1]	-40	+125	°C	Not supplied
13	P_{TOT}	Power dissipation		300	mW	
14	H_{max}	Maximum allowed applied magnetic field		10	kA/m	

[1] Packing materials such as tapes, reels, dry packs, foils, etc. are not considered. Please contact Sensitec GmbH for packing material specifications. Packaged devices before soldering: For moisture sensitive devices refer to JEDEC standard J-STD-033 for handling and using details. Storage temperatures > 90 °C for more than 96 h may affect the solder ability of the device.

4 ESD Protection

No.	Parameter	Description	Min.	Max.	Unit	Condition
1	$V_{PIN,ESDHBM}$	ESD HBM protection at all pins	2		kV	AEC-Q 100-002
2	$V_{PIN,ESDCDM}$	ESD CDM protection at corner pins	750		V	AEC-Q 100-011
3	$V_{PIN,ESDCDM}$	ESD CDM protection at all other pins	500		V	AEC-Q 100-011

5 Recommended Operating Conditions

The recommended operating conditions must not be exceeded in order to ensure proper functionality of the device. All parameters specified in the following sections refer to these recommended operating conditions if not otherwise stated.

All voltages referred to V(GND). Currents flowing into terminals are positive, those drawn out of a terminal are negative.

No.	Parameter	Description	Min.	Typ.	Max.	Unit	Condition
1	V_{SUP}	Supply voltage	4.75	5.0	5.25	V	
2	$(\Delta B/\Delta x)_{FS}$	Nominal range of magnetic flux gradient (for nominal output current I_{OUT})	-2.2		2.2	mT/mm	Permanent (DC) [1) 2)]
	$(\Delta B/\Delta x)_{2FS}$	Double flux gradient	-4.4		4.4	mT/mm	For maximum 3 s, and duty cycle < 1:10 [1)]
	$(\Delta B/\Delta x)_{3FS}$	Triple flux gradient	-6.6		6.6	mT/mm	For maximum 50 ms, duty cycle < 1:100 [1)]
3	T_{STG}	Storage temperature (not supplied)	-40		+85	°C	For less than 10 years
			+85		+125	°C	For maximum 5000 h during lifetime
4	T_J	Junction Temperature	-40		+125	°C	Normal operation
			+125		+150	°C	For max. 500 h over life time
5	R_{M_triple}	Load resistor between pins IOUT and FB	100	270	300	Ω	For triple output current range (I_{OUT})
	R_{M_nom}		300		900	Ω	For nominal output current range (I_{OUT})

1) Limitations to exposure times to magnetic field input (and resulting output) are due to the resulting power dissipation generated mainly by the sensor compensation current (see ch. 6.2.2) producing thermal heat inside the SO16w-package. Sensor calibrated in sensitivity.

2) Note: An excess homogeneous in-plane magnetic field in x- and y-direction (see fig, 1-1) superimposing the effective flux gradient should be kept below Bx,y < 0.6 mT by design of the application.

6 Functional Description and Electrical Parameters

6.1 Supply and References

6.1.1 Electrical Parameters

V_{SUP} = 4.75 V … 5.25 V, T_{AMB} = -40 °C … +125 °C, unless otherwise noted.
Typical values are at V_{SUP} = 5.0 V and T_{AMB} = 25 °C. Positive currents are flowing into the device pins.

Table 1: Supply and references block electrical parameters.

No.	Parameter	Description	Min.	Typ.	Max.	Unit	Condition
1	$I_{SUP(Q)}$	Quiescent supply current		23	28	mA	Zero field ($\partial B_x/\partial x = 0$) [2]
2	$V_{SUP(POR)}$	Power-on reset threshold	3.7		4.4	V	Falling supply
3	$V_{SUP(POR,HYS)}$	Power-on reset hysteresis	0.2		0.4	V	(Rising – falling) supply [1]
4	$V_{REFO,25}$	Internal reference output voltage @ room temperature	2.485	2.5	2.515	V	I_{REF} = ± 1.5 mA V_{REFI} < 0.3 V T_{AMB} = 25 °C
5	V_{REFO}	Internal reference output voltage	2.465		2.535	V	I_{REF} = ± 1.5 mA V_{REFI} < 0.3 V
6	dV_{REFO}	Load regulation internal reference	-3		+3	mV	V_{REFO} (I_{REFO}) - V_{REFO}(0) I_{REFO} = -1.5 ... +1.5 mA V_{REFI} < 0.3 V [1] [3]
7	$V_{REFI(TH)}$	Decision threshold for switching from internal to external reference at input REFI	0.5		1.0	V	Decreasing V_{REFI} until V_{REFO} increases from V_{REFI} to 2.5 V
8	$V_{REFI(RANGE)}$	Range of external reference	1.2	2.5	2.6	V	[1] [4]
9	$V_{REFO(OS),25}$	Offset voltage (REFO - REFI) @ room temperature	-5		+5	mV	V_{REFI} = 2.5 V I_{REFO} = 0 mA T_{AMB} = 25 °C
10	$V_{REFO(OS)}$	Offset voltage (REFO - REFI)	-5		+5	mV	V_{REFI} = $V_{REFI(RANGE)}$ I_{REFO} = 0 mA
11	$I_{REFI(LK)}$	REFI input leakage current	-1		1	µA	V_{REFI} = 2.5 V
12	t_{PON}	Power-on delay until output settled			4.0	ms	V_{SUP} surpasses 4.75 V I_{IOUT} settles to error band < 2% [1]
13	t_{INIT}	Initialization time from poweron to ASIFEN = 1	0.40	0.51	0.62	ms	See Figure 6-2
14	t_{ASIFEN}	ASIF activation time during start-up sequence	2.2	2.5	2.8	ms	See Figure 6-2
15	T_{OFF}	Over-temperature shut-down threshold	155		180	°C	Increasing T until OVC falls to 0 [5]
16	T_{HYS}	Over-temperature threshold hysteresis	10		30	°C	Decreasing temperature [5]

[1] Defined by design. Not subject to production test.

[2] Measurement condition: SETTH = REFI = 0 V; N_OVC = CDEL = REFO = open (hi-Z)
Note: The current consumption depends on sensor input (B-field). Typically, I_{SUP} increases by approximately 13 · | IOUT |

[3] Load capacitance $C_{REFO} \leq 1.5$ nF

[4] It has to be avoided by external circuitry when using an external reference, the voltage V_{REFI} could rise above the supply V_{SUP}.

[5] $T_{AMB} = T_J$ = +125°C, temperature thresholds calculated from voltage drop of diode circuit.

6.1.2 Description

This block includes voltage regulators for the excitation of the AMR-sensor bridge and to supply the internal digital and analog blocks of the signal conditioning IC. Both are generated from a precision bandgap voltage reference circuit. Also a buffer amplifier for the reference voltage output REFO which is selected from the internal voltage reference (bandgap) or an external reference input, a power-on reset monitor and an over-temperature monitor are part of this block.

6.1.2.1 Reference Voltage Generation

The IC includes an internal bandgap based reference voltage of 2.5 V (V2V5). An additional reference buffer feeds the reference to the output REFO in two different operation modes (see Figure 6-1):

- If $V_{REFI} < V_{REFI(TH)}$: buffering internal V2V5 to the output at pin REFO, or
- If $V_{REFI} \geq V_{REFI(TH)}$: buffering an external reference voltage applied at REFI to output pin REFO

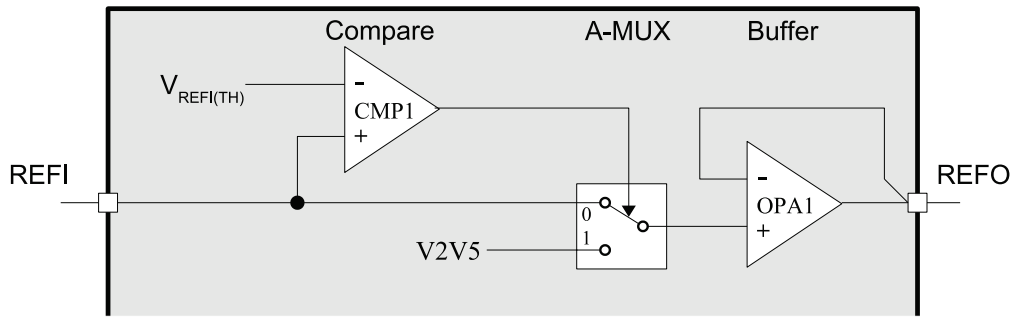


Fig. 6-1: REFO reference buffering.

This means, the input REFI is used simultaneously as a reference voltage input and for the level based decision which reference to be fed to the output.

At least two application cases for external reference voltage can be considered:

- Use a reference lower than the internal 2.5 V to define an asymmetric output signal (kind of “unipolar mode”)
- Use the same reference for several sensors to suppress the influence of mismatches of different references from different devices. E.g. in a 3-phase current measurement system the reference output REFO of one sensor can be used as input of the two other sensors or one very precise external reference would be used as input to all three sensor channels.

6.1.2.2 Reset Block

The IC contains an internal reset comparator, which observes the internal supply voltage. Due to the voltage drop at the regulator, the reset threshold $V_{PON} = V_{SUP(POR)} + V_{SUP(POR,HYS)}$ for rising supply voltage V_{SUP} shows a slightly wider spread than the threshold spread directly at the regulated voltage, but power up within the specified supply range is ensured. The reset comparator has a hysteresis $V_{SUP(POR,HYS)}$.

The general behavior of the reset block is depicted in Figure 6-2. With rising supply after V_{SUP} surpasses the power-on threshold, the IC copies the adjustment data from E²PROM to the corresponding data registers. This process is completed after t_{INIT}. Subsequently, for a duration t_{ASIFEN} the pins FB and IOUT are held in tri-state to allow for a log-in to the asynchronous programming interface (ASIF) via the pin FB, which is operated as a digital interface-I/O in this mode. This interface is described in more detail in another section below.

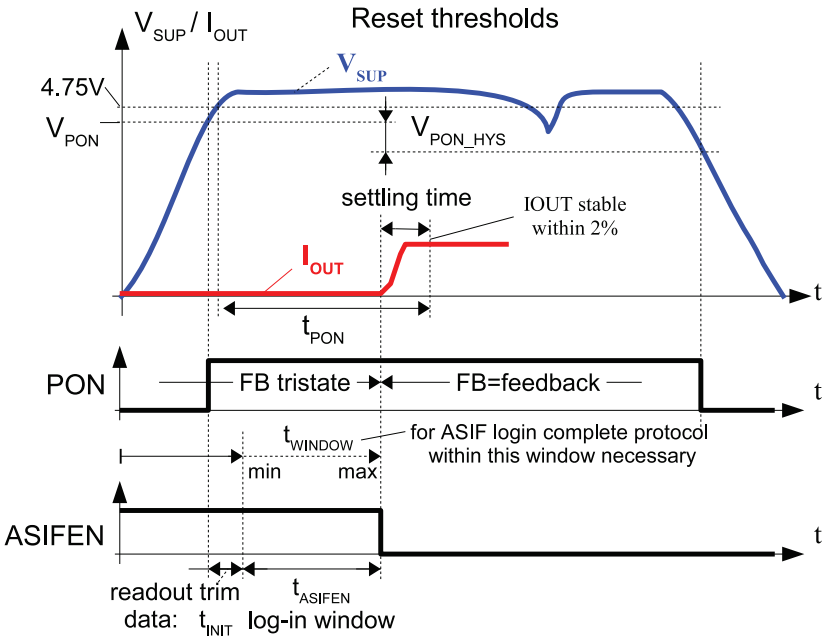


Fig. 6-2: Power-on timing and ASIF enable function.

During normal operation within the application the asynchronous interface (ASIF) will not be used and the IC enables pin FB for normal analog operation (after the t_{ASIFEN} is passed). If no log-in to the ASIF was executed, the IC-output IOUT settles to its final value with a certain precision within a power-on time t_{PON}, which is measured from the instant the supply V_{SUP} surpasses 4.75 V until the output has settled to a defined error band.

6.1.2.3 Over-temperature Monitor

To protect the IC from excessive heating by internal power sources a temperature sensor is integrated. If the junction temperature exceeds the temperature threshold T_{OFF}, the following actions are initiated:

- Compensation coil driver at pins IC1 and IC2 are switched off, and
- Due to the switch off of the compensation current also the output current I_{OUT} will be zero: $V_{IOUT} \approx V_{FB} \approx V_{REFO}$ (only differing by offset voltages in between), and
- Pin N_OVC output is pulled to Low

The over-temperature monitor has built in a hysteresis T_{HYS}, which ensures the IC can return to normal operation only, when the junction temperature has cooled down below $T_{OFF} - T_{HYS}$.

6.2 General Sensor Performance

6.2.1 Electrical Parameters

V_{SUP} = 4.75 V … 5.25 V, T_{AMB} = -40 °C … +125 °C, unless otherwise noted.
Typical values are at V_{SUP} = 5.0 V and T_{AMB} = 25 °C. Positive currents are flowing into the device pins.

Table 2: Sensor operating characteristics.

No.	Parameter	Description	Min.	Typ.	Max.	Unit	Condition
	Output characteristics						
1	$I_{IOUT(L)}$	Output low current drive capability	6	7		mA	V_{IOUT} = 0.5 V $V_{FB} = V_{REFO}$ + 100 mV [2) 14)]
2	$-I_{IOUT(H)}$	Output high current drive capability	6	7		mA	$V_{IOUT} = V_{SUP}$ – 0.5 V $V_{FB} = V_{REFO}$ – 100 mV [2) 14)]
3	V_{OUT}	Maximum output voltage range	0.5		4.5	V	V_{SUP} = 5 V, T_{amb} = 25 °C [2)]
4	BW	Signal bandwidth (-3 dB)	400	500		kHz	R_M = 330 Ω T_{AMB} = 25 °C [1) 2)]
5	t_{resp}	Response time		0.88	0.92	µs	90 % I_{PN} to 90 % $I_{OUT(FS)}$ [2) 15)]
6	t_{reac}	Reaction time		0.18	0.19	µs	10 % I_{PN} to 10 % $I_{OUT(FS)}$ [2) 15)]
7	t_{rise}	Rise time		0.75	0.79	µs	10 % $I_{OUT(FS)}$ to 90 % $I_{OUT(FS)}$ [2) 15)]
8	$V_{FB(OS)}$	Offset FB to REFO (closed-loop operation)	-5		5	mV	I_{IOUT} = 0 mA R_M = 330 Ω [2)]
9	PSR_{IOUT}	Power supply rejection PSR= ΔV_{SUP} / ΔV_{IOUT}	50			dB	R_M = 330 Ω $f_{SUP} \leq$ 5 kHz B_X = const. [1) 2)]
10	$R_{IOUT(PD)}$	Output load resistance	4.7			kΩ	IOUT to GND [2)]
11	$R_{IOUT(PU)}$	Output load resistance	4.7			kΩ	IOUT to SUP [2)]
	Pre-programming target (R_M = 330 Ω) [1)]						
12	$I_{IOUT(OS)PRE}$	Pre-programmed output offset current	-15 (-0.75%)		+15 (0.75%)	µA ($I_{OUT(FS)}$)	(ΔB/Δx) = 0 mT/mm V_{REFO} = 2.5 V [4), 12)] T_{AMB} = 25°C
			-25 (-1.2%)		+25 (1.2%)	µA ($I_{OUT(FS)}$)	T_{AMB} = 85 °C ...105 °C [2)]
			-20 (-1.0%)		+20 (1.0%)	µA ($I_{OUT(FS)}$)	T_{AMB} = 125 °C
			-35 (-1.7%)		+35 (1.7%)	µA ($I_{OUT(FS)}$)	T_{AMB} = -40 °C
13	$S_{X,PRE}$	Pre-programmed sensitivity		1.0		mA / (mT/mm)	T_{AMB} = 25 °C [3) 4)]
	Offset current output calibration (R_M = 330 Ω) [1)]						
14	$N_{OS,DAC}$	Offset current output calibration bits		8			[2)]
15	LSB_{OS}	Average current output step size (offset LSB value)		3.5	5.6	µA	Sensitivity = $S_{X,PRE}$ T_{AMB} = 25 °C [5)]
16	$ERR_{OUT(OS)}$	Offset current output calibration resolution	-0.85 (-4.8 µA)		+0.85 (4.8 µA)	LSB_{OS}	T_{AMB} = 25 °C [6)]
	Sensitivity calibration, Lateral field gradient in x-direction B_X = 2.0 mT/mm (R_M = 330 Ω) [1), 4)]						
17	$N_{GAIN,DAC}$	Sensitivity calibration bits		8			[2)]
18	LSB_{SX}	Step size of sensitivity calibration		0.3	0.5	% I_{OUT}	$I_{OUT} \approx$ 2 mA T_{AMB} = 25 °C
19	$S_{X,MAX}$ / $S_{X,MIN}$	Gain calibration range	1.67		2.0		T_{AMB} = 25 °C [7)]
20	S_X	Range of sensitivity trimming ensured by gain calibration	0.88	1.0	1.12	mA / (mT/mm)	T_{AMB} = 25 °C [4)]

No.	Parameter	Description	Min.	Typ.	Max.	Unit	Condition
	Output ranges and error components						
21	$I_{OUT(FS)}$	Nominal output range (after calibration)		±2.0		mA	(ΔB/Δx) = 2 mT/mm
22	$I_{OUT(PEAK)}$	Peak output range (after calibration)		±6.0		mA	(ΔB/Δx) = 6 mT/mm
23	TC_{Sx}	Thermal drift of sensitivity	-80		80	ppm/°C	T_{AMB} = -40 °C … +125 °C [2), 8)]
24	$\Delta I_{OUT(OS,REFI)}$	Offset shift due to variation of V_{REFI} (external reference, until offset re-calibration)	-15 (-0.75%)		+15 (0.75%)	µA ($I_{OUT(FS)}$)	(ΔB/Δx) = 0 mT/mm, I_{OUT}(1.2 V) – I_{OUT}(2.5 V), T_{AMB} = 25 °C [4), 13)]
25	$LIN_{ERR(NOM)}$	Linearity sensitivity error (nominal)	-6		6	µA	Nominal range: [2), 9)] $I_{OUT} = I_{OUT(FS)}$
26	$LIN_{ERR(PEAK)}$	Linearity sensitivity error (peak)	-30		+30	µA	Peak output range: [9)] $I_{OUT} = 3 \cdot I_{OUT(FS)}$
27	$I_{OUT(NOISE)}$	Output noise		2.5		$µA_{RMS}$	BW = 1 Hz - 500 kHz [2)]
				2.0		$µA_{RMS}$	BW = 1 Hz - 20 kHz [2)]
				0.5		$µA_{RMS}$	BW = 1 Hz - 1 kHz [2)]
	Overcurrent detection						
28	V_{SETTH}	Overcurrent detection threshold	0.5		V_{REFO} - 0.2	V	[2)]
29	$R_{SETTH(PU)}$	Pull-up resistor to supply	400	600	1000	kΩ	
30	$V_{OVC(HYS)}$	Overcurrent detection voltage hysteresis	20		100	mV	Rising edge N_OVC [2)] (back to passive)
31	$\Delta V_{IOUT(OVC)}$	Accuracy of overcurrent detection (voltage level)	-30		30	mV	V_{REFO} = 2.5 V [10)]
32	$V_{OVC(L)}$	OVC output low level			0.5	V	OVC detection active I_{OVC} = 5 mA
33	$R_{OVC(PU)}$	Pull-up resistor to supply	75	125	200	kΩ	
34	$t_{OVC(D,0)}$	OVC propagation delay, intrinsic delay			500	ns	Falling edge [2), 11)] C_{DEL} = 0 pF, V_{SETTH} = 1.0 V
35	$\Delta t_{OVC(D)}$	Additional OVC delay by use of CDEL capacitor	15	20	25	ns/pF	V_{SETTH} = 1.0 V [11)]
36	$t_{OVC(D,F)}$	Maximum delay (time-out) at OVC when CDEL at GND	10	15	20	µs	V_{CDEL} = 0 V

1) Output feedback IOUT to FB established with resistor R_M. It is recommended to use a low TC-type resistor R_M.

2) Defined by design. Not subject to production test.

3) Raw device characteristics before calibration.

4) Gradient of the magnetic field applied lateral in the sensor plane (x-direction, see Fig. 1-1) generated by the primary current.

5) Average current step size defined as { I_{IOUT}(D_OS = 0x7F) - I_{IOUT}(D_OS = 0x80) } / 254. (The spread of the average LSB results from sensitivity spread of the internal sensor).

6) Due to the differential non-linearity (DNL) of the offset-DAC (e.g. at MSB change) the residual error after offset calibration can be larger than the ideal 0.5 · LSB.

7) The ensured gain trimming range is tested between $S_{X,MAX}$ (D_GAIN = 0x70) and $S_{X,MIN}$ (D_GAIN = 0x80). The mid setting of gain is taken for D_GAIN = 0x00. Range extention to D_GAIN = 0x7F provides typically a 4.5% higher gain than D_GAIN = 0x70.

8) Temperature coefficient of sensitivity: $TC_{Sx} = \frac{S_x(T_2) - S_x(T_1)}{S_x(25°C) \cdot (T_2 - T_1)}$ with $T_1 = -40°C, T_2 = +125°C$

9) BFSL method (“best fit straight line”).

10) Overcurrent detection voltage level: $V_{IOUT(OVC)} = \mid V_{IOUT} - V_{FB} \mid - \mid V_{REFO} - V_{SETTH} \mid$

11) Delay time from passing the (absolute) threshold level defined by V_{SETTH} at IOUT and output falling below 1.0 V. Total delay is given by the sum of intrinsic delay and additional delay defined by capacitor at CDEL: $t_{OVC(D,0)}$ + CDEL · $\Delta t_{OVC(D)}$.

12) I_{OUT} can drift as much as ±20 µA (equivalent ±1% of nominal output $I_{OUT(FS)}$ = 2 mA) over the lifetime of this product.

13) When operated at reference levels different from the (internal) default of 2.5 V, an additional offset shift can occur due to the limited common rejection (CMR) of the amplifier. This offset shift can be canceled by re-calibration of the offset at V_{REFI}.

14) Indirect checked by output linearity check for range ±6 mA.

15) At nominal magnetic field gradient, di/dt = 380 A / µs, R_M = 330 Ω, T_{amb} = 25 °C; test setup with magnetic flux gradient of 2mT/mm and current increase to 20 A.

6.2.2 Description

By construction this AMR sensor is sensitive to magnetic field gradients in x-direction (parallel to the transversal axis of the IC). Therefore, current measurement in one conductor line requires the primary conductor to be fed forward and back below the sensor to create the differential field in the sensor plane ("U-shape"). The measurement based on evaluation of the magnetic field gradient (i.e. difference) makes the sensor insensitive to homogeneous magnetic stray fields superimposed. But, to ensure very good sensor performance magnetic field components in x- and y-direction in the sensor plane should be smaller than 0.6 mT. The base width of the magnetic sensor, i.e. the distance between the two legs of the magneto-resistive bridge, is 1.24 mm. The magnetic sensitivity orthogonal to the chip plane (z-direction) is negligible (see Figure 1-1 for a definition of the Cartesian coordinate system relative to the device in SO16w-package).

The principle of operation of the magneto-electrical loop as depicted in Figure 6-3 can be described as follows:

- The field (difference) H_{PRIM} generates a bridge output V_{IN} across the IC input pins INP and INM.
- This IC-input voltage V_{IN} is amplified ($G_1 \cdot G_2$) and corrected with adjustment inputs for offset and (linear) temperature coefficient of offset (TCO).
- This offset corrected output is amplified further amplified by (G_3) and V-I-converted by a transmission factor $1/R_{SENSE}$ into an output current I_{COMP}, which is then driven to the compensation wire of the sensor (resistance R_{COMP}).
- At the AMR sensor this compensation current I_{COMP} generates a differential magnetic field H_{COMP} with opposite polarity as the primary input field H_{PRIM} and thereby closes the (negative) feedback loop.
- Due to a high loop gain A_{LOOP} the primary input H_{PRIM} is perfectly compensated ($H_{COMP} = -H_{PRIM}$) and I_{COMP} is a highly linear representation of the primary input current I_{PRIM}.
- Finally, the output signal I_{OUT} is generated as a linear copy of the compensation current I_{COMP}. The reciprocal of this gain I_{OUT}/I_{COMP} in the following is denoted as "current copy ratio" FCC.

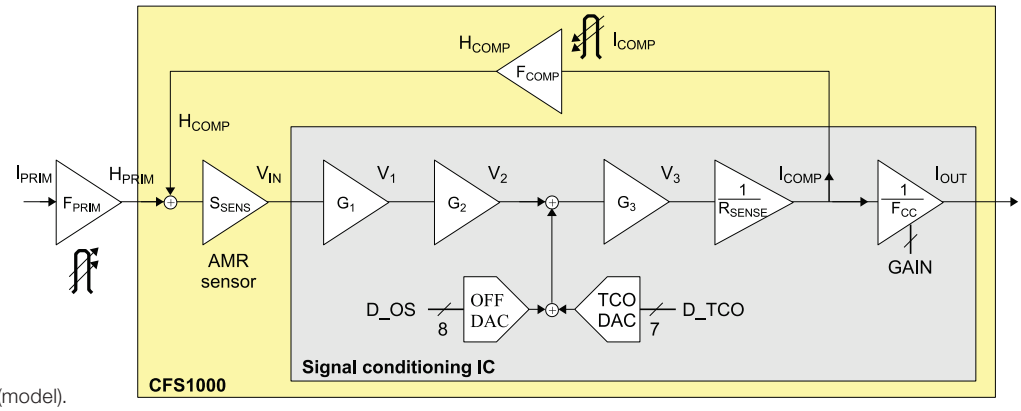


Fig. 6-3: Sensor signal path (model).

The following equations are used to describe the sensor transfer characteristic:

$$I_{OUT} = \frac{F_{PRIM}}{F_{COMP}} \cdot \frac{1}{F_{CC}} \cdot I_{PRIM} \quad \text{with} \quad A_{LOOP} >> 1$$

Where F_{PRIM} describes the coupling factor of primary current I_{PRIM} to magnetic field H_{PRIM} at sensor given by the geometry of the primary conductor beneath the sensor. According to Fig. 6-3, the loop gain is defined as:

$$A_{LOOP} = S_{SENS} \cdot F_{COMP} \cdot G_1 \cdot G_2 \cdot G_3 \cdot \frac{1}{R_{SENSE}}$$

(With the magnetic sensitivity of the bridge S_{SENS} and F_{COMP} being the sensor internal field coupling factor of I_{COMP}). Adjustment of system offset, offset thermal drift (TCO) and the gain (or sensitivity), respectively are described below.

6.2.2.1 Offset Adjustment

In Figure 6-3 two DA-converters are shown which are employed for trimming of the system offset and the temperature coefficient of this offset independently from each other. The major offset contribution is introduced by the AMR-sensor bridge itself, but also some offset contribution from the input amplifier of the signal conditioning IC exists.

The offset-DAC adds a multiple of a voltage LSB after the fixed gain input stages (G1 and G2) into the signal path, which is generated on-chip appropriately to the requirements of the sensor bridge. The resulting offset current at the output shows some minor parametric dependence on the sensor parameters (proportional to $1/[S_{SENS} \cdot F_{COMP}]$) due to the closed-loop structure described above (Figure 6-3). The corresponding output referred LSB is specified as LSB_{OS} (see ch. 6.2, Table 2). With an 8-bit calibration word, the resulting offset range with this LSB_{OS} is suited to calibrate for all expected offset contribution of sensor and amplifier path.

The value of the adjust byte D_OS[7:0] has to be interpreted as follows:

- D_OS[7]: sign of offset compensation (0 = positive; 1 = negative)
- D_OS[6:0]: unsigned integer with absolute value of offset compensation.

D_OS_{DEC}[6:0]	D_OS_{HEX}[6:0]	Output offset [1] $I_{OUT,OS}$ [µA]	
		D_OS[7] = 0	D_OS[7] = 1
0	0x00h	0	0
1	0x01h	+3.5	-3.5
2	0x02h	+7.0	-7.0
...	...	...	...
127	0x7Fh	+445	-445

[1] Typical values at 25 °C with sensitivity trimmed to nominal setting $SENS_{X,PRE}$ (see Table 2).

The table on the left gives an overview of the typical offset current setting as a function of D_OS[7:0]. The sensor CFS1000 is pre-calibrated to zero-offset by Sensitec's production sequence at component delivery, but it can be re-trimmed later in the application environment. For optimum accuracy it is recommended to perform a final calibration of offset and sensitivity (Chap. 6.2.2.2) together with a run-in sequence in an application environment. A second DAC for compensation of the offset drift in temperature (TCO) is used exclusively during Sensitec's production sequence to trim the overall offset drift to zero. This trimming module cannot be accessed regularly by the external programming interface (Chap. 6.6).

6.2.2.2 Current Output and Gain Adjustment

The output driver provides an output current between pins IOUT and FB which is proportional to the input signal. For conversion to voltage output a resistor R_M is connected from pin IOUT to FB.

As described above, as a consequence of the feedback employed, the compensation current I_{COMP} is a precise image quantity of the primary current I_{PRIM}, (generating a magnetic field, detected by the AMR sensor bridge). From this compensation current I_{COMP}, which is still quite large and cannot fit the necessary output range directly, an output current I_{OUT} is generated with a current copy function with constant "current copy gain" ($1/F_{CC}$) and high linearity, with FCC defined as:

$$F_{CC} = \frac{I_{COMP}}{I_{OUT}}$$ ("current copy ratio" = inverse of "current copy gain")

To compensate for process variations of the AMR bridge itself and to allow for a precise gain trimming, F_{CC} is adjustable with an 8-bit gain control DA-converter.

Figure 6-4 below depicts the simplified schematic of the current copy function. In a first stage (G5) the compensation current I_{COMP} is sensed by resistor R_{SENSE} and the drop is amplified and converted to a single-ended output. Then, a voltage-to-current converter (VIC) using op-amp OP1 generates the output signal I_{OUT}.

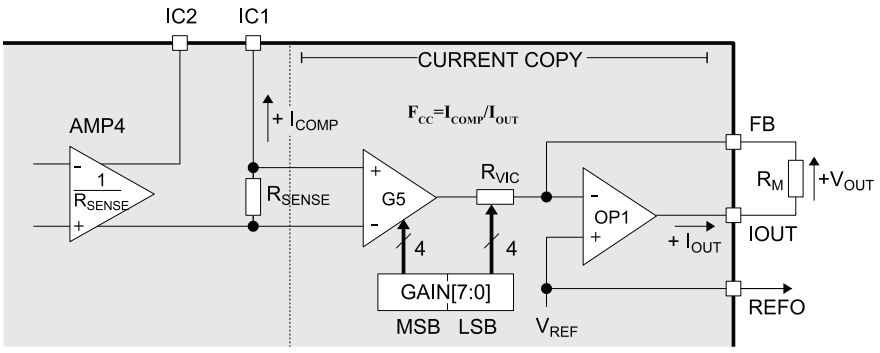


Fig. 6-4: Current copy schematic.

The programmable gain control realized as part of this block is distributed onto two 4-bit DACs:

- Most significant nibble GAIN[7:4] controls the gain of the differential amplifier G5 (“coarse gain trimming”)
- Least significant nibble GAIN[3:0] controls integrated resistor R_{VIC} (“fine gain trimming”)

Due to this distributed concept for trimming of the gain, the DAC characteristic may be neither totally monotone nor strictly linear, but a maximum adjustment step LSB_{SX} is defined which allows for a specified gain calibration precision.

Note: For precision applications it is recommended to adjust the gain only after assembly of the sensor device to the application, where the distance and relation to the primary current coil are mechanically fixed.

6.2.2.3 Overcurrent Alarm Output

For detection of an overcurrent violation two comparators are employed, which are observing the output level at pin IOUT. The overcurrent detection level is defined by the voltage level applied at pin SETTH. Both polarities of overcurrent are observed by this function, i.e. the overcurrent alarm output N_OVC is activated, whenever the absolute value of output current exceeds the limit defined by SETTH, as follows:

$$| I_{OUT} | = I_{OUT,max} > \frac{V_{REFO}}{R_M} \cdot \left(1 - \frac{V_{SETTH}}{V_{REFO}}\right)$$

Note: R_M denotes the feedback resistor connected between pins IOUT and FB

The detection level V_{SETTH} is most efficiently defined by a resistive divider to pin REFO (see Fig. 1-1). A pull-up resistor $R_{SETTH(PU)}$ between SETTH and REFO is integrated to cover cases where pin SETTH is high impedance erroneously (“open”). This would set the overcurrent threshold to zero, i.e. overcurrent alarm practically always on, and will avoid spontaneous alarm events generated at N_OVC due to a floating detection threshold. In the timing diagram below the behavior of the overcurrent alarm and definition of the detection thresholds is shown.

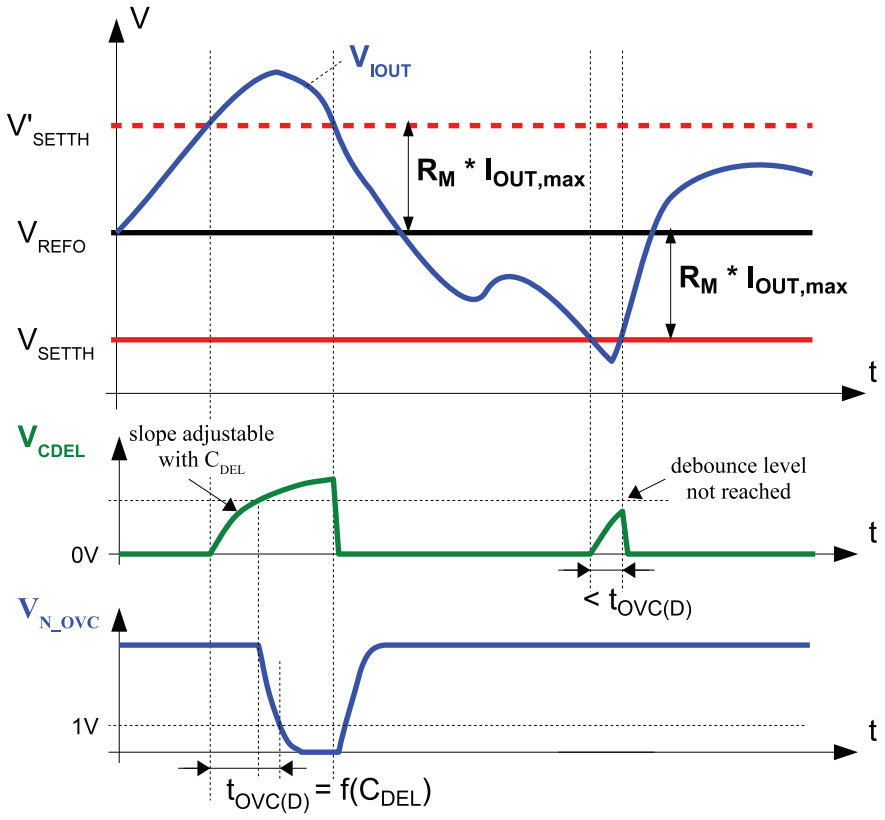


Fig. 6-5: Overcurrent alarm: thresholds and debounce behavior.

An additional debouncing delay which can be configured by connection of a capacitor to pin CDEL is implemented in the design of the overcurrent alarm. The delay can be calculated by the following approximation formula:

$$t_{OVC(D)} = t_{OVC(D,0)} + C_{DEL} \cdot \Delta t_{OVC(D)} \quad \text{with} \quad C_{DEL} = 50\,\text{pF}$$
$$t_{OVC(D)} \approx 0.5\,\mu\text{s} + 1.0\,\mu\text{s} = 1.5\,\mu\text{s}$$

Where $t_{OVC(D,0)}$ is the intrinsic delay and $\Delta t_{OVC(D)}$ the specific increase with a capacitor C_{DEL} connected (see Table 2). By this debouncing delay, alarm output events shorter than the delay time will be suppressed (not propagated to the alarm output N_OVC).
A maximum delay $t_{OVC(D,F)}$ (integrated time-out) ensures an overcurrent event will be propagated to N_OVC also in cases where CDEL is connected to GND erroneously.

Finally, an over-temperature event is logically combined (OR) to the alarm output N_OVC (see Chap. 6.1.2.3). An over-temperature event can be distinguished from overcurrent, by the output IOUT at zero and N_OVC pulled low.

The overcurrent alarm output is constructed as an open-drain driver as depicted in Figure 6-6. Although a pull-up resistor $R_{OVC(PU)}$ with quite high impedance is already integrated, it is recommended to use an external pull-up to the supply of the logic input connected (typically a few kΩ) to ensure a fast reaction of the alarm output.

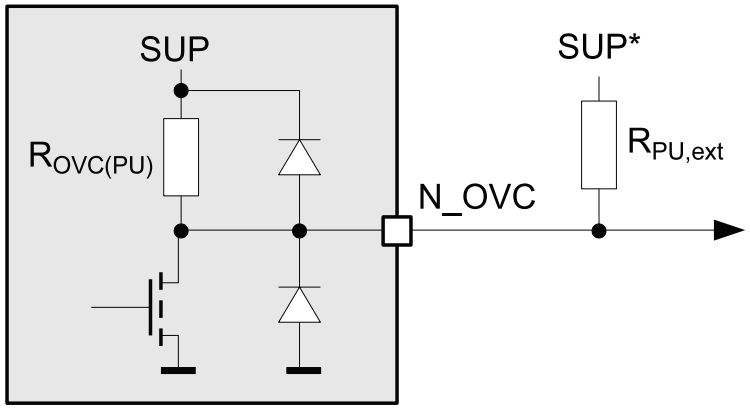


Fig. 6-6: Overcurrent output driver.

6.3 Typical Characteristics

The transfer function of the device is shown in Figure 6-7. For time limits for the 2 time nominal resp. 3 time nominal primary current I_{PN} refer to chapter 5.

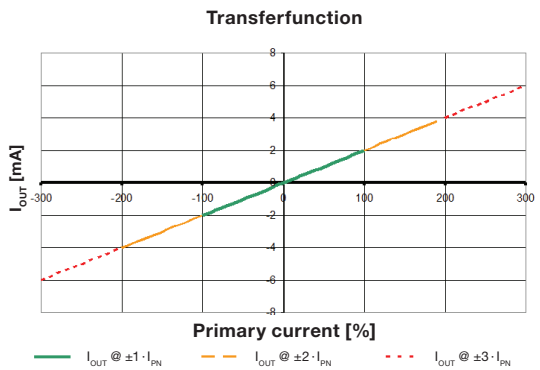


Fig. 6-7: Output signal I_{OUT} for nominal prim. current I_{PN} (green), 2 · I_{PN} (orange), and 3 · I_{PN} (red).

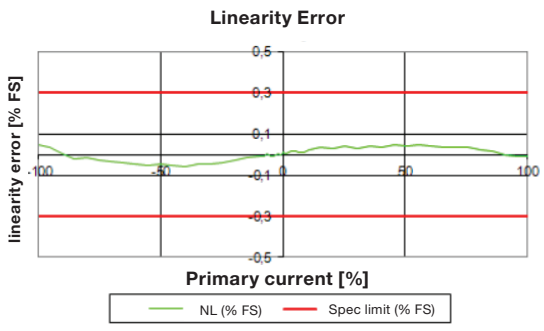


Fig. 6-8: Typical linearity error in primary current range.

Figure 6-8 shows the typical measured linearity error of a ±100 A application in % of the primary current. The red lines indicate the linearity sensitivity error specification limits from the section 6.2.1 Electrical Parameters.

6.4 Accuracy

The error bands for offset and sensitivity error are shown in Figure 6-9 and Figure 6-10. The deviations are referred to the values at 25 °C.

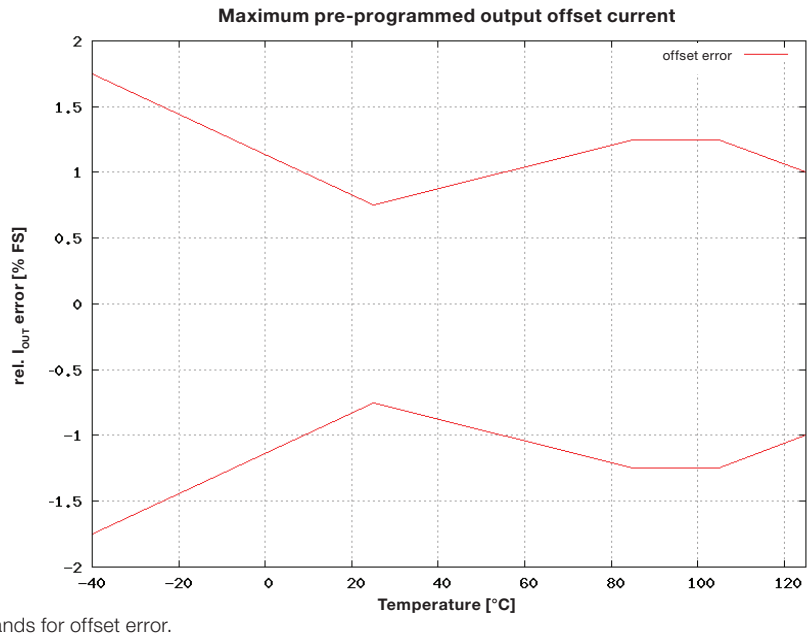


Fig. 6-9: Specified error bands for offset error.

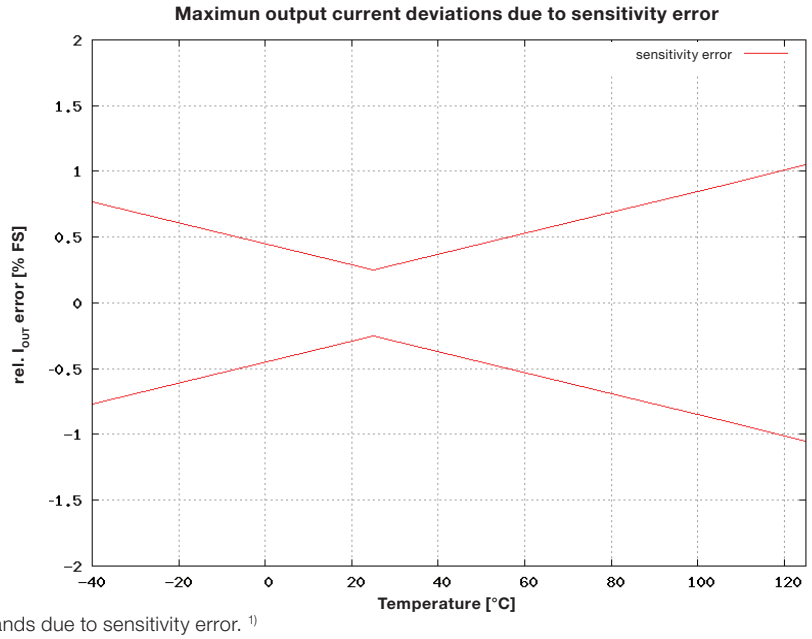


Fig. 6-10: Specified error bands due to sensitivity error. [1)]

1) Impact from thermal properties of application, e.g. PCB materials not included.

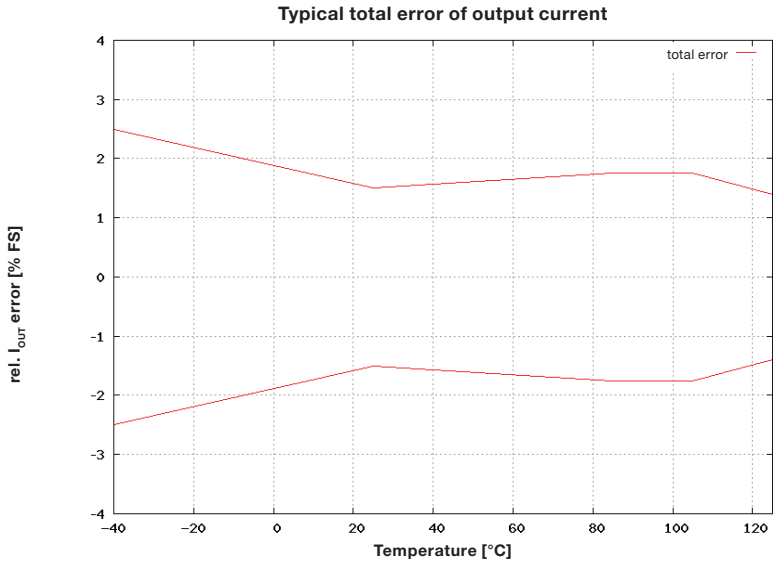


Fig. 6-11: Typical maximum range of total error after calibration. [1), 2)]

1) Impact from thermal properties of application, e.g. PCB materials not included.

2) Based on a weighted superposition of contributions from gain, offset, linearity and temperature dependence.

6.5 E²PROM

6.5.1 Electrical Parameters

V_{SUP} = 4.75 V … 5.25 V, T_{AMB} = -40 °C … +125 °C, unless otherwise noted.
Typical values are at V_{SUP} = 5.0 V and T_{AMB} = 25 °C. Positive currents are flowing into the device pins.

Table 3: E²PROM data retention parameters

No.	Parameter	Description	Min.	Typ.	Max.	Unit	Condition
1	N_{PROG}	Number programming cycles	1000			1	$T_J \leq 125$ °C [1)]
2	t_{DR1}	Data retention [1), 2)]	20			yr	$T_J \leq 85$ °C
3	t_{DR2}		3			yr	85 °C ≤ T_J ≤ 105 °C
4	t_{DR3}		1			yr	105 °C ≤ T_J ≤ 125 °C
5	t_{DR4}		500			h	125 °C ≤ T_J ≤ 150 °C

1) Defined by design. Not subject to production test. E²PROM is qualified according to AEC-Q100, grade 0

2) Figures specified are guaranteed data retention times at the given temperature and must not be cumulated. For a specific temperature profile in operating life time (OLT), the specific exposure times for cumulation can be calculated on demand by Sensitec GmbH.

6.5.2 Description

The IC contains an E²PROM memory for application specific calibration data (GAIN & OFFSET) and further adjustment data (TC-Offset and IC-specific adjustments). Only the lower 4 bytes (address 0x00h ... 0x03h) of this NVM are generally accessible via the ASIF (see section 6.6), while the addresses above 0x03h are read-only and cannot be modified after Sensitec GmbH production test sequence.

After power-on, the E²PROM bytes for the adjustment information bits are read out and copied into the corresponding registers. Table 4 summarizes the memory mapping of the E²PROM (general accessible section).

Table 4: E²PROM register allocation

EEPRROM address	Register name	Access	Description
0x00h	FREE0	R/W	unused register (free use for application data)
0x01h	FREE1	R/W	unused register (free use for application data)
0x02h	OFFSET	R/W	Offset adjustment (8 bit), internal name: D_OS
0x03h	GAIN	R/W	Sensitivity adjustment (8 bit)

6.6 Programming Interface and Digital Controls

6.6.1 Electrical Parameters

V_{SUP} = 4.75 V … 5.25 V, T_{AMB} = -40 °C … +125 °C, unless otherwise noted.
Typical values are at V_{SUP} = 5.0 V and T_{AMB} = 25 °C. Positive currents are flowing into the device pins.

Table 5: Programming interface electrical parameters.

No.	Parameter	Description	Min.	Typ.	Max.	Unit	Condition
1	$R_{FB(PU)}$	ASIF pull-up resistor at FB	1.8	3.3	5.3	kΩ	ASIFEN = 1
2	$V_{FB(IN,HI)}$	ASIF input Hi level at FB	4.0		V_{SUP}	V	ASIFEN = 1
3	$V_{FB(IN,LO)}$	ASIF input Lo level at FB	0.0		0.8	V	ASIFEN = 1
4	$V_{FB(OUT,LO)}$	ASIF output Lo level at FB	0.0		0.5	V	I_{FB} = 1 mA, ASIFEN = 1
5	$R_{rsv(PD)}$	Pull-down resistor at pins rsv1, rsv3	14	20	26	kΩ	
6	$V_{rsv(HI)}$	Digital input Hi level at pins rsv1, rsv3	4.1		V_{SUP}	V	
7	$V_{rsv(LO)}$	Digital input Lo level at pins rsv1, rsv3			0.8	V	
8	t_{IF_DLY}	Delay between enabling ASIF (ASIFEN = 1) via rsv1 / rsv3 and start of 1st protocol	110			µs	Rising edge rsv1 / rsv3 to 1st falling edge at FB See Figure 6-15 [1]
9	$C_{FB(LD)}$	Load capacitance during ASIF-operation (interface)			150	pF	[1]
10	t_{BIT_RX}	Valid ASIF bit length for receiving at pin FB	85	100	115	µs	see Figure 6-16
11	t_{HBIT_RX}	Valid ASIF half bit length for receiving	0.45	0.50	0.55	t_{BIT_RX}	see Figure 6-16
12	t_{RX}	Length of valid receiving protocol	- (0.94)	11 (1.10)	- (1.26)	t_{BIT_RX} (ms)	see Figure 6-18
13	t_{BIT_TX}	ASIF bit length for transmitting at pin FB	90	100	110	µs	see Figure 6-16
14	t_{HBIT_TX}	ASIF half bit length for transmitting	0.47 (42)	0.50 (50)	0.53 (59)	t_{BIT_TX} (µs)	see Figure 6-16
15	t_{TX}	Length of transmission protocol	- (0.98)	11 (1.10)	- (1.22)	t_{BIT_TX} (ms)	see Figure 6-18
16	t_{FB_rise}	Digital input rise time at pin FB for RX and TX			2	µs	from 20% to 80% [1]
17	t_{FB_fall}	Digital input fall time at pin FB for RX and TX			2	µs	from 80% to 20% [1]
18	t_{RX_DLY}	Valid delay between reception of two protocols	3 (330)			t_{BIT_TX} (µs)	see Figure 6-18
19	t_{TX_DLY}	Delay between command protocol and response	2 (180)		3 (330)	t_{BIT_TX} (µs)	see Figure 6-18
20	t_{PRG_DLY}	Delay between data protocol and confirmation protocol after programming	16		21	ms	see Figure 6-18

[1] Defined by design. Not subject to production test.

6.6.2 Description

A digital state machine controls the complete IC and provides the following functions:

- ASIF (asynchronous serial interface) as data interface for calibration in the application and data read-back
- E²PROM control (NVM for storage of calibration data)
- Read-out of calibration data from E²PROM to the corresponding registers after power-on
- Control of the test interface and test modes (Sensitec GmbH dedicated production test; restricted access)

This chapter concentrates on the description of the ASIF and its use as the most important feature for the application of the CFS1000. Because this interface uses the pin FB as digital I/O it is not possible to run the normal sensor application simultaneously in the programming mode via ASIF. This implies, the calibration measurements required to determine the calibration data (GAIN, OFFSET) need to be done in a sequence with the data I/O via ASIF.

6.6.2.1 Calibration Adjustment

For the specified precision of the AMR current sensor in its application environment, the IC CFS1000 needs adjustment. Therefore, the respective adjustment data are stored during the calibration process in an integrated E²PROM (non-volatile memory = NVM).

The adjustment can only partially be done before packaging or assembly of the device into its application environment. Especially the GAIN-adjustment determining the precise sensitivity of the CFS1000 is recommended to be executed after soldering the device in order to ensure precise mechanical fixing with respect to the primary current conductor. Optionally, also the final trimming of the OFFSET can be done in this phase, while other calibration data (e.g. thermal coefficient of the offset) are completely performed during the sensor production test sequence at Sensitec GmbH.

For E²PROM programming an asynchronous serial interface (ASIF) is implemented, which uses the pin FB as a bidirectional digital-I/O. To enter the interface mode (ASIFEN = 1: “interface enabled”) just after power-on during a certain time interval an ASIF-command has to be sent to FB. This interval with ASIFEN=1 opens after t_{INIT} for the login time t_{ASIFEN} (see Figure 6-2, Table 1) and the login command (0xD5, see Table 6) has to be transmitted completely in this interval. In the time directly after power-on the pin FB does not operate as an analog I/O as described above (section 6.2.2.2), but as a digital I/O with an integrated pull-up $R_{FB(PU)}$. If the IC is transmitting, an open-drain low-side driver is employed to drive the logic Low level (Figure 6-12). A similar structure is recommended to drive data the ASIF (receivemode RX).

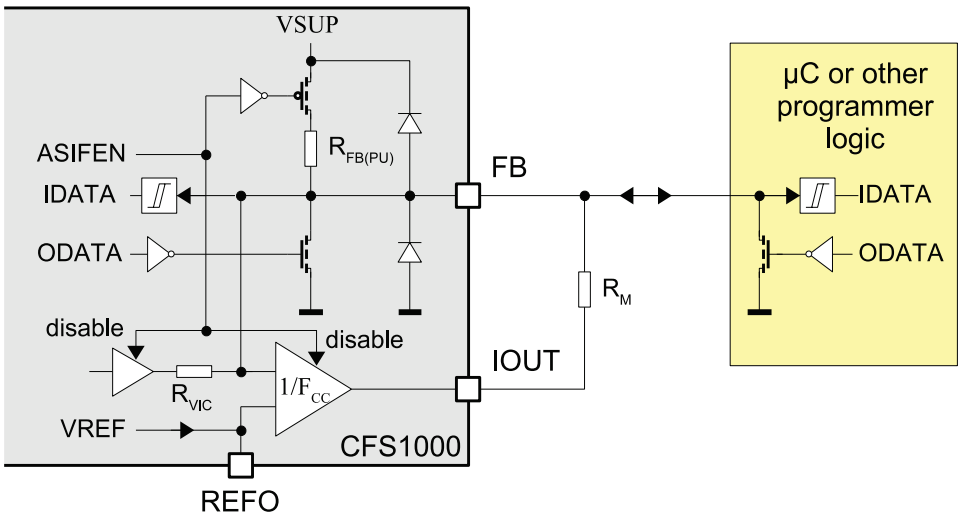


Fig 6-12: Asynchronous serial interface (ASIF), circuit concept.

Because of the low-impedance connection between FB and IOUT in the application circuit (normal sensor operation), also the output driver at IOUT is switched to high impedance during “ASIF active” (ASIFEN = 1) to allow for safe data transmission into FB (RX-mode).

In Figure 6-13 below an exemplary application circuit is depicted which can be employed to adjust the CFS1000 via ASIF. Because this interface uses the pin FB, it is not possible to operate simultaneously the normal sensor application mode during ASIF-programming mode and vice versa. Because log-in to ASIF mode is possible only after power-on a quite fast reset, which is operated synchronously to the external programming logic is needed.

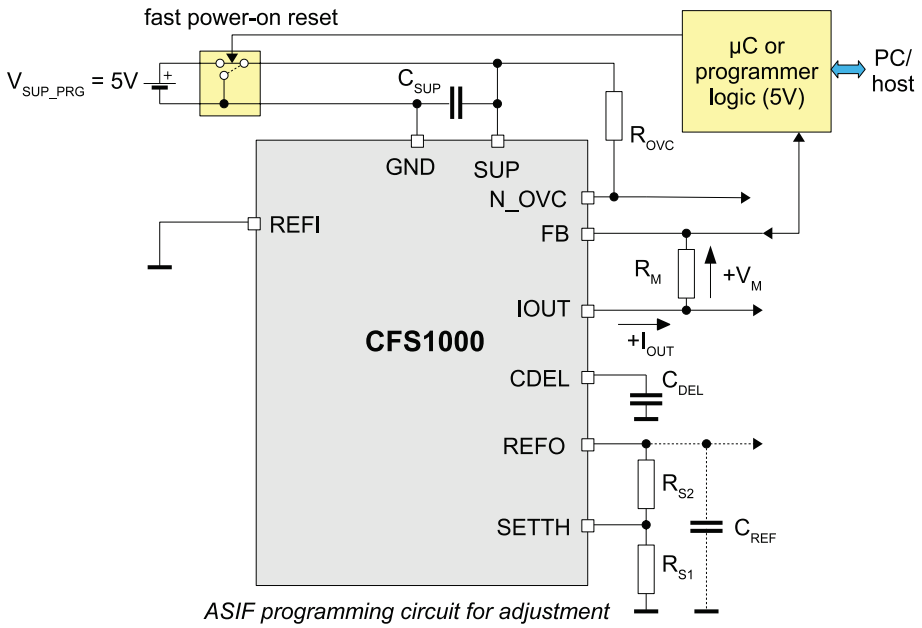


Fig 6-13: ASIF Programming Circuit.

If also access to the test interface pins rsv1, rsv3 is available, the alternative programming circuit example depicted in Figure 6-14 should be be used. Rather than using a power-on reset via supply pin SUP, to enable the ASIF the pins rsv1 and rsv3 need to be pulled to logic high level simultaneously.

On the other hand, the pull-up of pins rsv1 and rsv3 has to be avoided imperatively during normal operation, because it would immediately affect the regular analog circuit function at pins IOUT / FB.

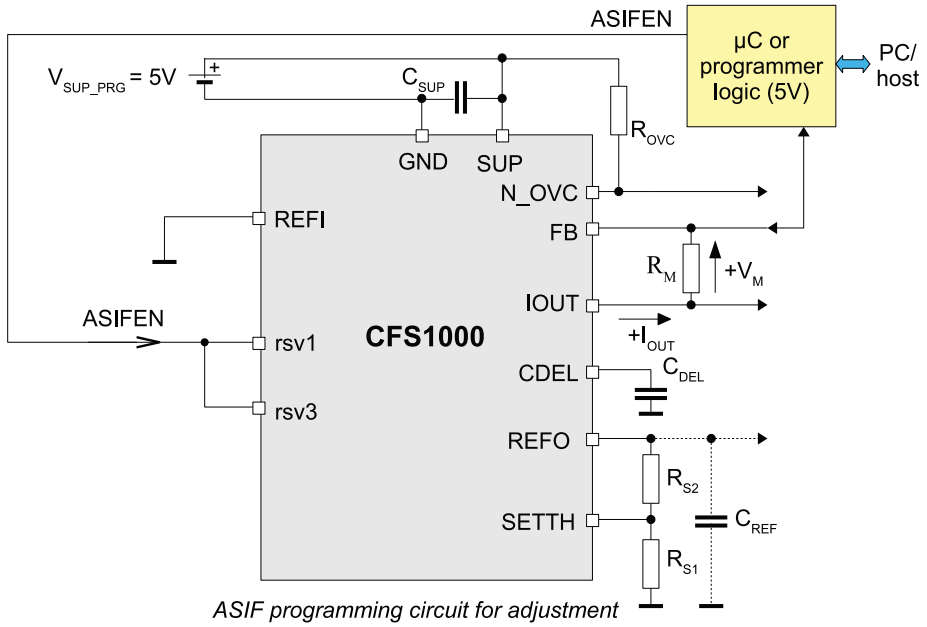


Fig 6-14: ASIF Programming Circuit; using reserved input pins.

In Figure 6-15 below the log-in timing to enter ASIF-mode is depicted when access to pins rsv1 and rsv3 is possible. No restricted time interval after power-on needs to be observed here, but only a minimum wait time t_{IF_DLY} before data transmission may start is to be ensured. The ASIF remains active as long as pins rsv1 and rsv3 are kept at logic high level.

During data communication via ASIF the load capacity $C_{FB(LD)}$ at pin FB must be limited to meet the specified timing (see Table 5).

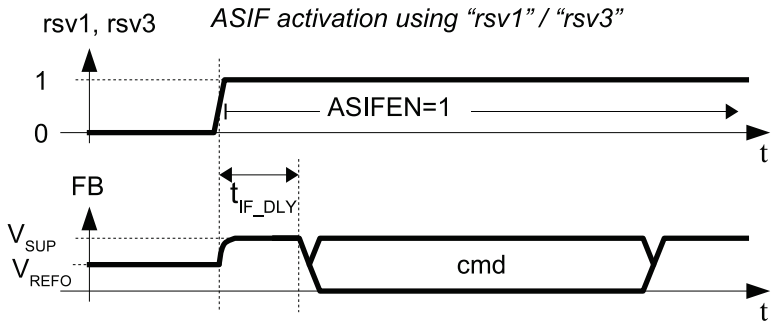


Fig 6-15: Log-in to ASIF with access to pins rsv1 and rsv3.

6.6.2.2 ASIF Protocol and Encoding

This sub-chapter describes the bit coding and the protocol construction of the ASIF. Manchester coding is used for data transmission as shown in Figure 6-16. The necessary timing parameters for receive (RX) and transmit (TX) are specified as $t_{BIT\_RX/TX}$, $t_{HBIT\_RX/TX}$, t_{FB_rise} and t_{FB_falll} (see Table 5).

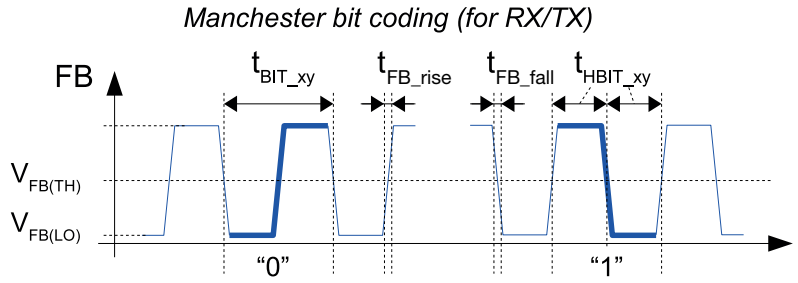


Fig. 6-16: Manchester bit coding and bit timing for transmit and receive.

The transmission protocol consists of 11 bits in total: 2 start-bits followed by 8 data bits or command bits, and 1 parity bit which indicates the end of a protocol. The command or data byte within the protocol starts with MSB first. An example for read out of an ID-byte is shown in the picture below (Figure 6-17). In case of a parity failure (i.e. no odd parity detected within all 11 bits), or a start-bit-error, or any other error be detected, within a protocol frame, the protocol will be ignored.

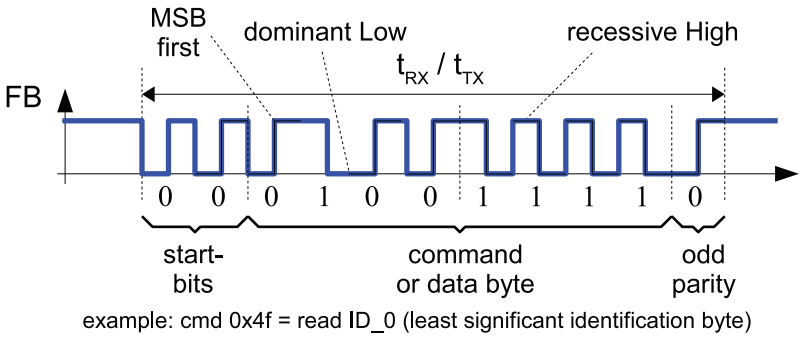


Fig. 6-17: ASIC protocol format and example.

6.6.2.3 ASIF Commands

The ASIF-commands consist of a sequence of 2 or 3 interface protocols as described in the last section. Two general types of ASIF-commands are depicted in Figure 6-18 below.

Each ASIF-command starts with a command byte send from an external logic to the CFS1000. In the first command format shown in Figure 6-18 the IC response contains the requested data, or a confirmation data byte, if no data requested.

The second command format is used for E²PROM programming. Here, the command includes the E²PROM address and is followed by the data byte to be programmed to the E²PROM of the CFS1000. After an interval t_{PRG_DLY} required for E²PROM-programming, the IC transmits the data byte read back from the corresponding E²PROM address to the programming module externally connected at the ASIF interface.

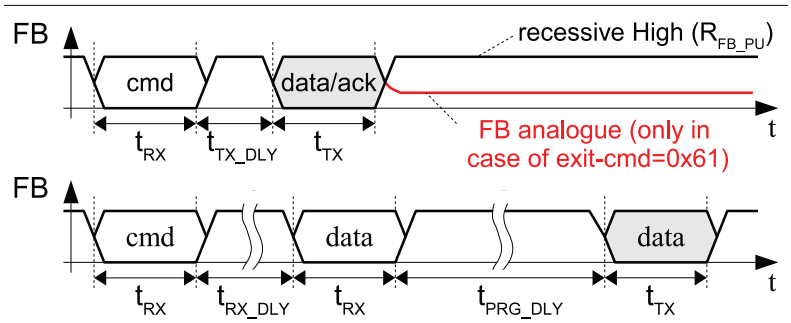


Fig. 6-18: ASIF command format overview.

The specified time delays t_{TX}, t_{RX}, t_{PRG_DLY}, t_{TX_DLY}, and t_{RX_DLY} (see Table 5) have to be considered for proper communication in order to avoid the pin FB is driven simultaneously from the external and the integrated transmitter. Hard driver conflicts are avoided by defining this interface as Low dominant / High recessive, i.e. open-drain drivers with pull-up resistor.

The table below summarizes the ASIF-commands which are implemented in the IC of the CFS1000.

Table 6: ASIF-commands overview.

Code	ASIF-instruction	Next I/O-operation	3rd I/O-operation
0x4Y	Read E²PROM address <Y> [1]	TX read out data byte	None
0x51	Write unused E²PROM byte	RX data byte to program	TX read back data byte
0x52	Write OFFSET	RX data byte to program	TX read back data byte
0x53	Write GAIN	RX data byte to program	TX read back data byte
0x60	Update all adjustment registers from E²PROM	TX confirmation data byte **0x00**	None
0x61	Exit programming mode to application mode	TX confirmation data byte **0x01**	None
0xD5	Log-in to programming mode	TX confirmation data byte **0x05**	None (programming mode is entered, FB at “High” with pull-up)
All other	(undefined command)	TX confirmation data byte **0xE1** or **0xE2** [2]	None

[1] Wildcard “Y” stands for any address 0x00 ... 00xF of the E²PROM memory map (see Table 4).

[2] Depending on the code of the “undefined command”, two different error codes are sent

Note: TX = transmit from IC to external modules; RX = IC receives protocol data.

7 Package Information

The CFS1000 is available in a Pb free, RoHs compliant, SO16w plastic package according to JEDEC MS-013-F, variant AA.

The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260 + 5) °C.

Note: Thermal resistance junction to ambient $R_{TH,JA}$ is 80 K/W, based on standard JESD-51-7.

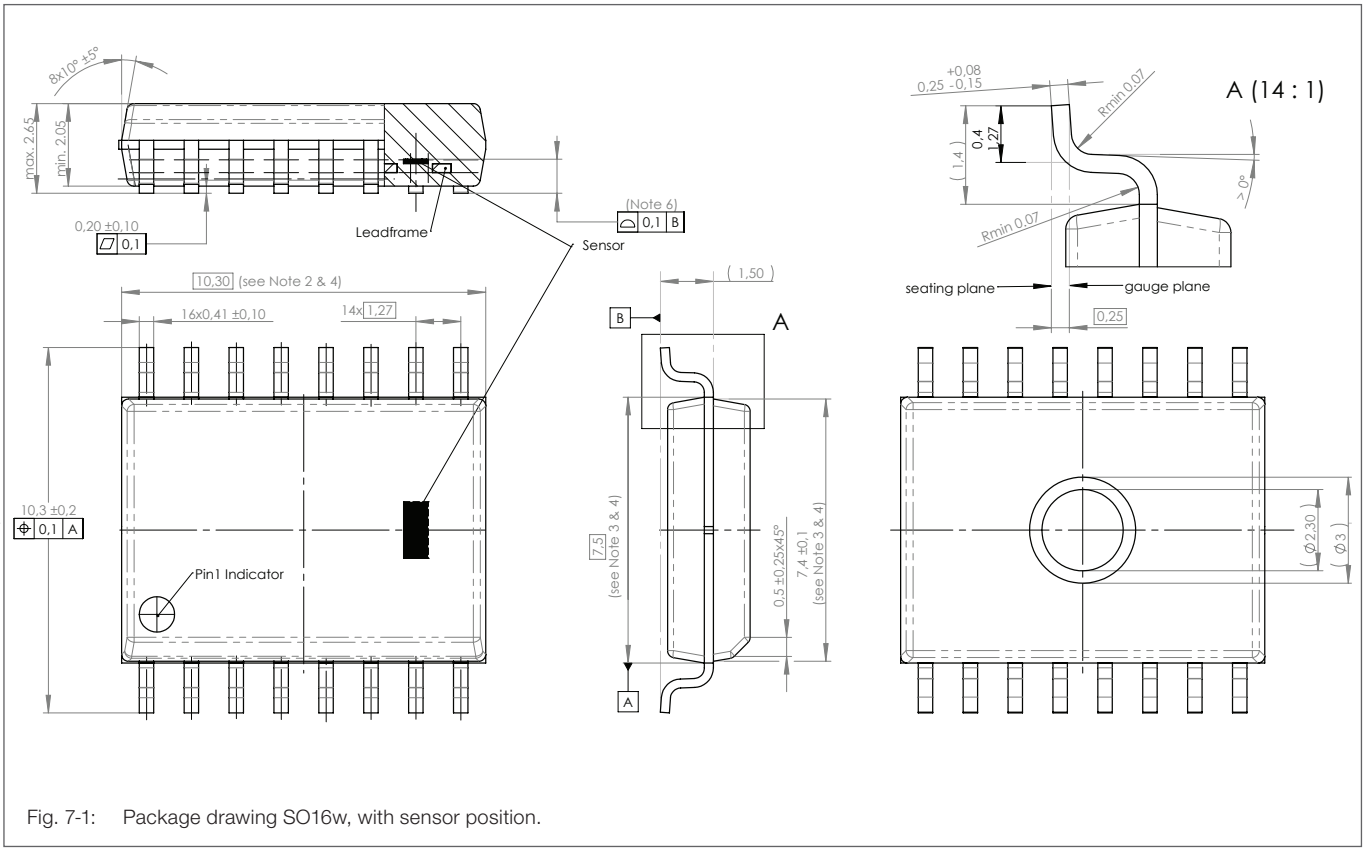


Fig. 7-1: Package drawing SO16w, with sensor position.

Notes:

1. Package outline and dimensions are according JEDEC MS-013-F, variant AA.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exeed 0.15 mm per end.
3. Dimensions does not include interlead flash or protrusion. Interlead flash or protrusions shall not exceed 0.25 mm per side.
4. The package top may be smaller than the package bottom. Both dimensions are determined at the outermost extremes of the plastic body, exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Leadframe is Tin plated. No visible evidence of bare Cu, caused by clamping or bending during lead froming. Plating thickness is 0.3 to 1 mils (7.62 to 25.4 microns).
6. Assuming a sensor thickness of 0.26 mm, the distance of the sensor to ground can vary between 0.94 mm - 1.27 mm worst case.
7. Position of sensitive area in x is indicated by connecting line between pins 7 and 10; position in y is centered around the middle axis of the package, vertical position of sensitive area is typically 1.1 mm above seating plane of the package.
8. All Dimensions in mm.

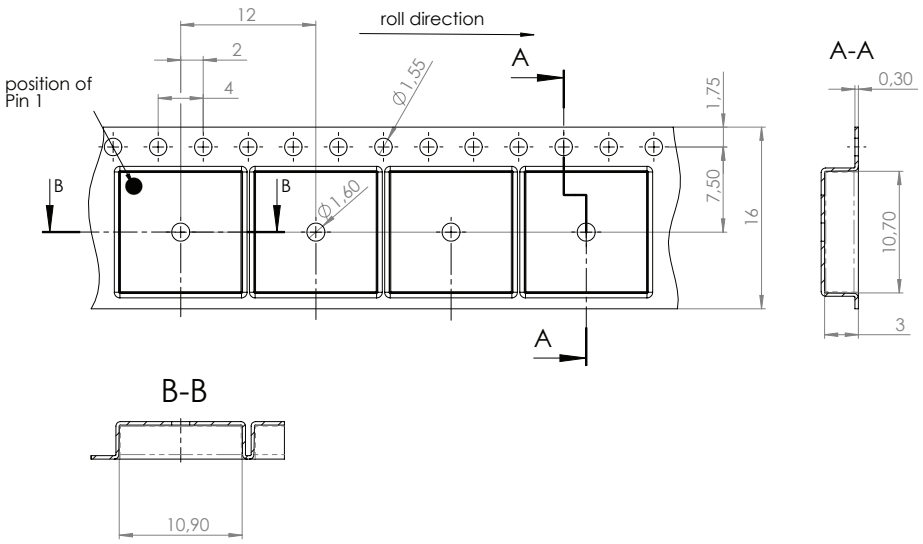


Fig. 7-2: CFS1000 tape on reel.

Notes:

1. The tape on reel is compliant to DIN/IEC-60286-3:2014-02, type 2a.
2. Nominal reel diameter: 330 mm.
3. One reel contains max. 1500 parts.
4. All dimensions in mm.

General Information

Product Status

Article	Status
CFS1000AAA-AE	The product is in series production.
Note	The status of the product may have changed since this data sheet was published. The latest information is available on the internet at www.sensitec.com.

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Sensitec GmbH
Schanzenfeldstr. 2 · 35578 Wetzlar · Germany
Phone +49 6441 5291-0 · Fax +49 6441 5291-117
www.sensitec.com · sensitec@sensitec.com